REMARKS

Claims 1-27 are currently pending and subject to examination. No amendments to the claims have been made by this response.

I. Claim Rejections under 35 U.S.C. § 102

Claims 1-14 and 19-23 stand rejected under 35 U.S.C. § 102(e) as being unpatentable over U.S. Patent No. 6,694,464 to Quayle, et al. (Quayle). This rejection is respectfully traversed, as follows.

Claim 1 is directed to a method including dividing pins of an integrated circuit into a first group and a second group, logically associating each pin of the first group to each pin of the second group, and generating a scan chain in the integrated circuit for each logical association of pins.

In contrast, Quayle is directed to a hardware emulation system which reduces hardware cost by time-multiplexing multiple design signals onto physical logic chip pins and printed circuit board. See abstract. As shown in Fig. 1, multiplexed signals from a first mux chip are transmitted to a logic chip. Multiplexed signals from the logic chip are then transmitted to a second mux chip. As shown in Fig. 11, the mux chips also have connections to a backplane connector 220 and a turbo connector 202. The turbo connector 202 is used to electrically connect two logic boards 200 together in a sandwich.

The Office Action seems to suggest that the connections between the backplane pins to the mux chips, and the connections between the turbo pins and the mux chips, are considered to be a logical association of pins, which the Applicants do not concede. However, even if the

connections to the mux chips were considered to be a logical association, each of the pins in the backplane connector would not be associated with each of the pins in the turbo connector.

Quayle uses a partial crossbar interconnect, in which the input/output pins of each logic chip are divided into proper subsets, using the same division on each logic chip. The pins of each mux chip are connected to the same subset of pins from each logic chip. Thus, each of the pins connects only to one mux board, so that, for example, as shown in Fig. 11, the first mux board receives information only from the first third of the pins in the backplane connector and from the first third of the pins in the turbo connector. As shown in Fig. 1, the first logic chip receives information only from the second mux chip, and transmits information only to the first mux chip. Thus, even if the connections were considered to be logical associations, Quayle would not teach or suggest logically associating **each pin** of the first group to **each pin** of the second group."

In contrast, claim 1 of the present invention recites the limitation "logically associating each pin of the first group to each pin of the second group." As Quayle does not teach or suggest this limitation, claim 1 is patentable over the art of record.

Claims 6, 10, and 19 recite similar language to claim 1 and are patentable for similar reasons to those discussed above with reference to claim 1. Dependent claims 2-5, 7-9, 11-14, and 20-23 are dependent on independent claims 1, 6, 10, and 19, respectively, and are patentable for at least those reasons discussed above with reference to the independent claims.

I. Claim Rejections under 35 U.S.C. § 103 and Statement of Common Ownership

Claims 15-18 and 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Quayle. Applicants note that, at the time the claimed invention was made, the claimed invention and the subject matter of Quayle were owned by, or were subject to an obligation of assignment to, the same person.

Specifically, at the time the claimed invention was made, the claimed invention was owned by, or was subject to an obligation of assignment to, Cadence Design Systems, Inc. Enclosed please find an Assignment Recordation Form showing the assignment of the claimed invention to Cadence Design Systems, Inc. Furthermore, at the time the claimed invention was made, Quayle was owned by, or subject to an obligation of assignment to, Quickturn Design Systems, Inc., a wholly owned subsidiary of Cadence Design Systems, Inc.

As this Statement of Common Ownership disqualifies Quayle as prior art under 35 U.S.C. 103, withdrawal of the rejection of claims 15-18 and 24-27 is respectfully requested.

CONCLUSION

Based on the foregoing, all claims are believed allowable, and an allowance of the claims is respectfully requested. If the Examiner has any questions or comments, the Examiner is respectfully requested to contact the undersigned at the number listed below.

If the Commissioner determines that additional fees are due or that an excess fee has been paid, the Patent Office is authorized to debit or credit (respectively) Deposit Account No. **50-2518**, billing reference no. **7034222001**.

Respectfully submitted,
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